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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,231	12/04/2001	Alain Benayoun	FR920000052	8295

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EXAMINER	
LAM, DANIEL K	
ART UNIT	**PAPER NUMBER**
2667	2

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,231	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Daniel K Lam	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-13* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 to 8 are objected to as failing to comply with 37 CFR 1.84 because descriptive labels that are necessary for understanding the drawings, are missing.
2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

- On page 4:
    - In paragraph 21, numerals 13-1 to 13-4 and 15-1 to 15-4 are mentioned but are missing in fig. 1.
    - In paragraph 22, numeral 200 is mentioned but is missing in fig. 2.
    - In paragraph 25, symbols EXPIN-1 to EXPIN-8 are mentioned but are missing in fig. 2.
    - In paragraph 26, EXPOUT-1 to EXPOUT-8 are mentioned but are missing in fig. 2.
- On page 6, paragraph 32, request_for_connection, grant_connection, and general_back_pressure signals are mentioned but are missing in fig. 3.
- On page 7, paragraph 37, General_Back_Pressure, Queue_Status, Synchronization signals are mentioned but are missing in fig. 4.
- On page 8:

- In paragraph 42, numerals 203-1 to 203-8 and 207-1 to 207-8 are mentioned but are missing in fig. 7.
- In paragraph 43, symbols Exp1_1, Exp2_1, Exp1_2, Exp2_2, Exp1_3, and Exp2_3 are mentioned but are missing in figures 8A and 8B.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

4. The abstract of the disclosure is objected to because the form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a

whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Pat. No. 5,166,926 issued to Cisneros et al. in view of the paper, titled, "Application Brief: Allayer Rox Bus Architecture", by Allayer Communications.

Regarding claims 1, 8, and 10, while patenting the high speed packet switch, Cisneros et al. discloses the limitations of a switching module for switching LAN traffic in a data transmission system comprising:

a) An INPUT MODULE 260(1) having INPUT LINE 245(1) I(1) that receives user data and stores them into QUEUE 505 (First receiver which stores a first plurality of data packets; claims 1, 8, and 10). See fig. 5, and col. 18, lines 47-54, and col. 21, lines 20-23.

b) An INPUT MODULE 260(1) having INPUT LINE 245(1) I(2) that receives user data and stores them into QUEUE 505 (Second receiver which stores a second plurality of data packets; claims 1, 8, and 10). See fig. 5.

c) An OUTPUT MODULE 270(1) having OUTPUT LINE 275(1) O(1) that transmits user data (First output which outputs a first subset of the first plurality of data packets and the second plurality of data packets; claims 1, 8, and 10). See fig. 5, col. 32, lines 18-20, and col. 33, lines 60-61.

d) An OUTPUT MODULE 270(1) having OUTPUT LINE 275(1) O(2) that transmits user data (A second output which outputs a second subset of the first plurality of data packets; claims 1, 8, and 10). See fig. 5.

e) A SELF-ROUTING CROSS-POINT PLANE 550(1) switch coupled to the first receiver and the second receiver and coupled to the first output and the second output for routing the first subset and the second subset to the respective first or second output (claims 1, 8, and 10). See fig. 5, col. 20, lines 7-14 and lines 38-40.

However, Cisneros et al. does not disclose limitations that the first and second switching modules are connected such that first expansion data-out circuit of the first switching module is connected to a first expansion data-in circuit of the second switching module, and a first expansion data-out circuit of the second switching module is connected to a first expansion data-in circuit of the first switching module (claim 8).

Allayer Communications discloses the limitations of linking two crossbars together so that the number of output ports can be expanded. See page 5, first paragraph, lines 1-3, bottom figure on page 7, "Port Linked (not Stacked) Switches", and top figure on page 8, "Linking two crossbars (not stacking)".

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to stack the switching modules so that the number of ports can be increased without having to exponentially increase the number of switching modules as taught by Allayer Communications; see page 4, lines 24-25.

Regarding claim 2, in addition to disclose the limitations regarding claim 1 discussed in the previous paragraphs, Cisneros et al. further discloses the limitations that the switch module comprises:

a) A plurality of STS-3c INPUT LINES 245 that are connected to a plurality of INPUT MODULE[s] 260 for receiving user input data (a set of `m` data-in circuits for receiving the first plurality of data packets from a plurality of LAN adapters); see fig. 5, and col. 15, lines 4-7.

b) Each individual INPUT MODULE 260, such as INPUT MODULE 260(1), contains a BUFFER MEMORY 1030 for storing ATM cells that are received from INPUT LINE[s] 245(1) and 245(2) (each data-in further comprising: a first memory for storing the first subset of said first plurality of data packets, and a second memory for storing the second subset of said first plurality of data packets); see fig. 10, and col. 30, lines 29-36.

c) A multiplex MUX 1020 for selecting when and where to store the ATM cells into the BUFFER MEMORY 1030 (a selector for sending each received frame of said first plurality of data packets either to the first memory or the second memory); also see fig. 10, and col. 30, lines 29-36.

Regarding claims 3, 6, and 7, in addition to disclose the limitations regarding claim 2 discussed in the previous paragraphs, Cisneros et al. further discloses the limitations that the INTERFACE MODULE 210(1) prepends an APPENDED SWITCH ROUTING HEADER 120 to each received ATM cell. The APPENDED SWITCH ROUTING

HEADER 120 consists of 8-bit OUTPUT MODULE PHYSICAL ADDRESS 127 AND 5-bit OUTPUT MODULE PORT ADDRESS 123. By physically assigning an address to each OUTPUT MODULE 270, received ATM cells can be routed from any input port in the INPUT MODULE 260(1) to any output port in any OUPUT MODULE 270 (Each ATM data packet comprising an additional byte to define the final destination of said data packet, said additional byte including a module bit configuration to determine in which of said first or second memory the data packet is to be stored; claim 3. An address configurator for predefining the address of the switch module; claim 6. The address of the switch module is a bit configuration to be compared to the module bit configuration of each incoming data packet; claim 7). See figures 1 and 2, col. 7, lines 38-44, and col. 13, lines 6-13.

Regarding claims 4 and 5, in addition to disclose the limitations regarding claim 3 discussed in the previous paragraphs, Cisneros et al. further discloses the limitations that:

a) Each output module, such as OUTPUT MODULE 270(1), routes the incoming ATM cells to one of the separated OUTPUT PORT[s] O(1) to O(n) (First output comprises a set of `p` data-out circuits for receiving the first subset of first plurality of data packets and the second plurality of data packets; claim 4. Second output comprises a set of `n` expansion data-out circuits for receiving the second subset of first plurality of data packets; claim 5); see fig. 5, and col. 20, lines 57-61.

b) The demultiplexor, DEMUX 1240, routes cell to one of the output port (A controller to route the first subset of first plurality of data packets and the second plurality of

data packets to the appropriate data-out circuit according to the additional byte configuration; claim 4); see fig. 12, and col. 33, lines 53-60.

c) The incoming ATM cells are written into CELL BUFFER 1233 situated within BUFFER MEMORY 1230. Separated logical queue is assigned to each output link (Storage for storing the second subset of said first plurality of data packets received from the corresponding data-in circuit; claim 5). See fig. 12, and col. 32, lines 54-62.

Regarding claim 11, in addition to disclose the limitations regarding claim 10 discussed in the previous paragraphs, Cisneros et al. further discloses the limitation that the STS-3c frame is received by the INPUT MODULES 260 located within the SWITCH FABRIC 250. The frame is then divided into ATM packets (each frame comprising a plurality of data packets). See col. 15, lines 4-7.

Regarding claims 12 and 13, while patenting the high-speed packet switch, Cisneros et al. discloses a method for routing a plurality of data packets in a data transmission system, comprising the steps of:

a) Receiving data packets from the first INPUT MODULE 260(1). See fig. 5, and col. 18, lines 47-54.

b) The INTERFACE MODULE 210(1) prepends an APPENDED SWITCH ROUTING HEADER 120 to each received ATM cell. The APPENDED SWITCH ROUTING HEADER 120 consists of 8-bit OUTPUT MODULE PHYSICAL ADDRESS 127. The cell is routed to one of the OUTPUT MODULE[s] 270 by comparing the

physical address of the output module located in the header against the physical address of the OUTPUT MODULE 270 (Comparing the final destination address of each of said data packets to a switch module address range of the first switching module; claim 12. Assigning a switch module address range to each switching mode; claim 13). See figures 1 and 2, col. 7, lines 38-44.

c) Allayer Communications further discloses the limitations of stacking crossbars in order to expand the number of ports. See page 5, first paragraph, lines 1-3, bottom figure on page 7, "Port Linked (not Stacked) Switches", and top figure on page 8, "Linking two crossbars (not stacking)".

Allowable Subject Matter

7. Claim 9 is objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel K. Lam whose telephone number is (703) 305-8605. The examiner can normally be reached on Monday-Friday from 8:30 AM to 4:30 PM.

   If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone number for this Group is (703) 872-9314.

   Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

dkl

DKL: February 23, 2004

Chau T. Nguyen

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